Quasi-Digital CMOS Temperature Sensor for on-Chip Thermal Monitoring of Self-X Systems

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Abstract

This paper presents a simple and fully integrated small size CMOS temperature sensor with quasi digital output for on-chip temperature monitoring. The proposed circuit converts the linear temperature-dependent current of the proportional to absolute temperature (PTAT) biasing circuit into a frequency signal by exciting a simple current-mode relaxation oscillator (RO). In order to reduce the circuit area, a current-mode comparator is used in the design of the RO. The post-layout simulations show that under the worst-case process corners and $\pm 10\%$ supply voltage variation, the temperature sensor has a maximum absolute nonlinearity error of 2.4°C for the temperature range from -40 °C to $+85$ °C with a power figure of merit equal to $0.2 \frac{\mu W}{kHz}$. The circuit occupies a layout area of 0.028 mm^2. The circuit is designed using the XFAB 0.35 μm technology and Cadence Virtuoso tools for verification and physical implementation.

1 Introduction

The ability to integrate densely packed transistors in advanced node process and system-on-chip (SoC) technology increased system intelligence and computation speed at the price of higher power consumption. Consequently, generating more heat and raising the die temperature may cause permanent thermal damage or, less aggressively, performance and power efficiency degradation at elevated temperatures [1, 2, 3]. Furthermore, high on-chip temperature leads to increase the leakage currents, which in turn rise the chip power dissipation [4]. Standalone traditional cooling techniques using off-chip solutions like heat-sinks, fan air cooling, or even sophisticated solutions like microfluidic cooling systems are inadequate to maintain chip safety in modern integrated circuits (ICs) [5, 6]. Therefore, an on-chip thermal management system [7] is necessary and established by now to locally and effectively track the chip temperature to prevent chip overheat malfunction or dynamically optimize system performance accordingly by using evolvable hardware (EHW) mixed-signal electronics with self-X properties (self-calibrating, self-adapting, etc.) [8, 9]. Therefore, the chip lifecycle will be enhanced [10] because its reliability is highly correlated to the temperature [11].

To have a comprehensive thermal measurement profile, several temperature sensors can be spread at different chip locations, especially near the more subjected heat areas that create dangerous hot spots [12, 13]. Hence, this highlights the need for the low area and low power consumption temperature sensor design [14]. The latter demand also reduces the self-heating of the sensor elements that can cause inaccuracy measurement error [15]. Various types of CMOS monolithic temperature sensors utilize the temperature dependency of the CMOS elements, e.g., resistors, parasitic BJTs (bipolar junction transistors) and MOSFETs. Generally, the BJTs based temperature sensors have high linearity that enables them to support high-resolution temperature measurement but consumes more area [16].

A common temperature measurement procedure in these types of sensors is by comparing the complementary to absolute temperature (CTAT) voltage of the base-emitter junction (V_{BE}) or the proportional to absolute temperature (PTAT) difference voltage between two non-equal size junctions (ΔV_{BE}) to a temperature-independent reference voltage [17]. The ratio between CTAT/PTAT voltage to the reference voltage representing the measured temperature is converted to digital using analog-to-digital converter (ADC) [18]. To reduce the area and power consumption related to the use of ADCs, the sensor output can be realized in a quasi-digital domain that modulates temperature quantity in the form of period, frequency, pulse number, time interval or duty cycle [19], followed by time/frequency to digital converter, which consumes less area and power [13, 16, 20].

A recent work in [21, 22] incorporates this principle by exploiting the temperature dependency of the MOS resistors and MOS transistors, respectively. However, the accuracy and resolution of this approach significantly depend on the quality of the clock signal; additionally, the MOSFETs solutions are less linear than BJTs counterparts [23]. Authors in [24] avoided using the clock by designing a temperature sensor based on an asynchronous counter to count the number of generated pulses as a function of temperature. An intermediate solution is followed by authors in [25, 26] by using the BJTs and time to digital conversion to achieve small size, low power, and high accurate temperature sensor design. In smart sensory electronics [8, 9, 27], the microcontroller/digital processing unit can be employed to perform the quasi-digital to digital conversion of the temperature sensor with high resolution granted by the accurate timers of the processing unit. Hence, make

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it an attractive choice to simplify the sensor design further as implemented in [28].

Nevertheless, the quasi-digital sensors are becoming more prominent owing to their main features of combining the simplicity of the digital signals and the noise immunity of analogue sensors [29, 30]. This paper aims to design a quasi-digital temperature sensor for on-chip thermal management based on high linear ΔV_{BE} PTAT current properties of the parasitic BJTs in CMOS 0.35 μm technology. Section 3 presents the proposed schematic circuit, while the layout and the post-layout simulation results are presented in section 4. Section 5 report briefly the achieved results.

2 Proposed Temperature Sensor

The proposed circuit schematic is depicted in figure 1 consists mainly of two units; the first unit represents the temperature sensing core (TSC) which perform the temperature to current conversion. The second unit is the current-controlled oscillator (CCO) that execute the temperature-dependent current to frequency conversion. The TSC is a bandgap reference circuit (BGR) that produce a PTAT current (I_{PTAT}) and also generates the reference trigger voltage (V_{GR}) for the comparator in the CCO stage. The I_{PTAT} is mirrored to the CCO to generate a quasi-digital signal, modulating the temperature change in frequency with a constant duty cycle of 50%. The BGR circuit is constructed using wide swing cascode mirrors (M1-M12) to improve the current matching and to have a high power supply rejection ratio (PSRR) at the cost of only two additional BJTs (Q1, Q4).

Although regular cascoded mirrors are a more straightforward solution, keeping the cascoded transistors in the saturation region is challenging against the worst case of process, voltage and temperature (PVT) variations in standard 3.3 V CMOS technology. An alternative solution is by boosting the mirror impedance using an auxiliary differential amplifier with simple current mirrors. Overall, the latter solution leads to larger layout area and addresses the amplifier stability issue.

The PTAT current is defined by [31]:

$$I_{PTAT} = \frac{V_{BE2} - V_{BE1}}{R_1} = \frac{V_T \cdot \ln(m)}{R_1} \tag{1}$$

where V_T is the bipolar thermal voltage, and m is the size ratio between Q3 to Q2 transistors and fixed to eight in this design.

The temperature coefficient (TC) of the generated PTAT current can be derived as:

$$TC(I_{PTAT}) = \frac{1}{I_{PTAT}} \cdot \frac{\partial I_{PTAT}}{\partial T} \tag{2}$$

$$TC(I_{PTAT}) = \frac{1}{V_T} \cdot \frac{\partial V_T}{\partial T} - \frac{1}{R_1} \cdot \frac{\partial R_1}{\partial T} = TC(V_T) - TC(R_1) \tag{3}$$

Because the first term of equation 3 has a positive TC ($\frac{\partial V_T}{\partial T} \cong 0.086\text{mV}/^\circ\text{C}$), a sheet resistor with a higher negative TC helps to increase the $TC(I_{PTAT})$, consequently the sensor sensitivity ($S = \frac{\partial I_{PTAT}}{\partial T}$) will also increase. On the other hand, the second-order component of the $TC(R_1)$ introduces unwanted nonlinearity error to sensor measurement at high and low T. Hence, a poly resistor with the smallest available negative TC has been selected from the used technology. The I_{PTAT} is designed to be 5 μA at room temperature as a trade-off choice between the power dissipation and the resistor size defined by the sheet resistance. Another vital consideration toward reducing I_{PTAT} is to avoid the resistor's self-heating effect which add an offset error to the measured temperature.

The CCO circuit is a CMOS type current-mode relaxation oscillator [32] that also use a simple current-mode comparator (M21-M23) adapted from [33] to generate clock type signal by comparing the capacitor voltages to the reference voltage (V_{BGR}). With high enough gain of the comparator, the output oscillated thermal dependent signal frequency can be approximated to:

$$f_{OSC} = \frac{1}{T_{OSC}} = \frac{I_{PTAT}}{2C_{1,2}V_{BGR}} \tag{4}$$

because in the design, $C_1 = C_2$ and are charging with the same amount I_{PTAT} and compared to equal trigger voltage (V_{BGR}), the duty cycle of the output signal is almost 50%. The V_{BGR} is not designed to have a minimum possible TC as in the prevalent case of the BGR circuits. In this design, the TC of the V_{BGR} is tuned by adjusting the R_2/R_1 ratio during simulation to compensate for the residual nonlinearity effect of both the TSC and CCO units. Because The TC of the used MIM capacitor is very small and can be ignored, the output clock signal has PTAT characteristics with linearity dominated by the linearity of the PTAT current.

It is possible to generate the clock signal using only one capacitor, as authors did in [33]. However, in this case, the capacitor must be completely discharged to zero before the next charging cycle starts. Hence, it is required to delay the decision of the latch circuit using a delay circuit and using a fast discharging switch to the ground. Although the delay circuit is not complex and can be implemented using a chain of inverters and capacitors, the delay time dependency on the PVT condition can introduce an error to the signal frequency. The latter problem can be reduced by using a larger capacitor, increasing the design size. Also, it is possible to use the very basic current starved oscillator [34] to convert the PTAT current to a frequency; however, this type of circuit has a voltage supply dependency.

Finally, the transistors (M28-M33) represent the necessary startup circuit of the BGR. A slight modification has been introduced to the work presented in [35] , wherein this paper, startup sinking and sourcing currents are injected into the BGR upper and lower mirrors respectively to guarantee a safe startup under the worst PVT conditions. The dynamic startup currents go to zero after the BGR successive initiation, therefore, it has no impact on the I_{PTAT} characteristics. The MOSFETs size ratios of the proposed circuit are listed in table 1 and designed to fit the circuit functionality under worst-case conditions with smallest possible area.

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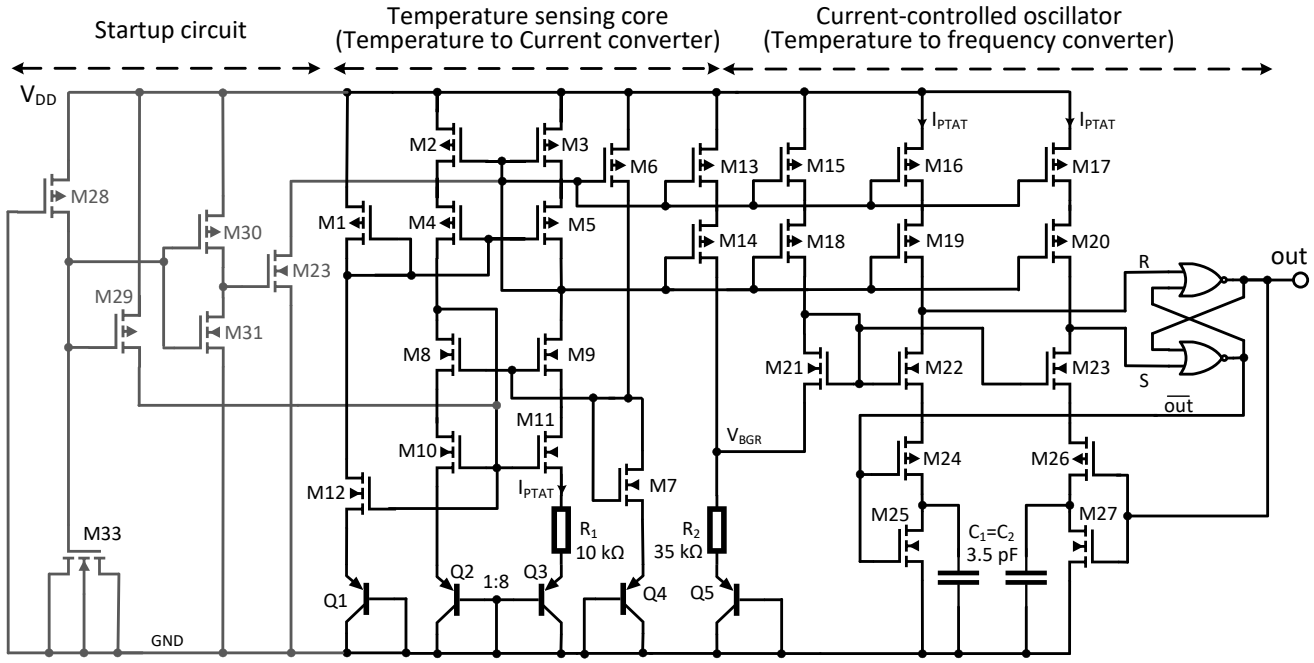

Figure 1 The proposed temperature sensor schematic circuit using the XFAB 0.35 μm technology.

Table 1 MOSFET size ratios of the proposed sensor circuit

Tr. Nr.	(W/L) [μm/μm]	Tr. Nr.	(W/L) [μm/μm]
M1	30/8	M13	120/2
M2-M6, M15-M20	60/2	M14	120/2
M7	10/8	M24, M26	6/0.35
M8-M12, M21-M23	20/2	M25, M27, M30	2/0.35
M28	0.5/24	M29	5/0.35
M31	1/0.35	M32	5/0.35
M33	30/30		

3 4. Layout Implementation and Post Layout Simulation Results

In addition to using high impedance mirrors with a channel length of 2 μm, the common- centroid layout technique is followed during the layout design to improve the current matching. The circuit layout is shown in figure 2 consumes only 0.028 mm^2.

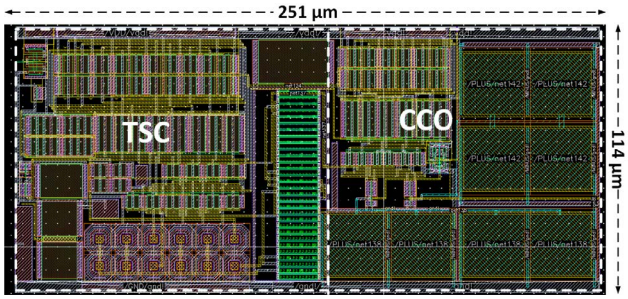

Figure 2 Physical implementation of the proposed temperature sensor.

The sensor post-layout output characteristics is presented in figure 3 under all process corners, while the nonlinearity error is derived and given in figure 4 based on the best-fit line calculation. The worst-case nonlinearity error was found to be -2.467 °C at the WP corner and supply voltage of 3 V. The average sensitivity of the sensor ($\frac{\partial f_{OSC}}{\partial T}$) at nominal conditions (V_{DD}=3.3 V and typical mean process) is 1.957 $kHz/$°C.

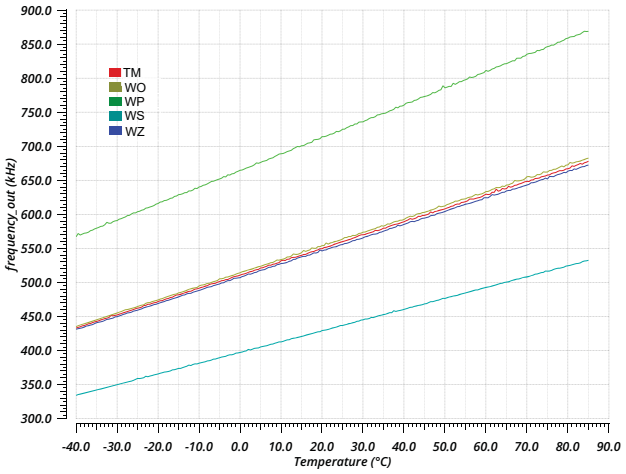

Figure 3 Temperature sensor output characteristics at VDD= 3.3 V and all possible process corners (TM: typical mean process, WP: worst-case power, WS: worst-case speed, WO: worst-case one, WZ: worst-case zero).

The change in the output frequency with the process corners is due to the process effect on sheet resistance which leads to change I_{PTAT} as shown in figure 5 , and also the same effect on the capacitance. The sensor power dissipation is proportional to the output frequency at the relevant temperature with a figure of merit equal to 0.2 $\frac{\mu W}{kHz}$ under

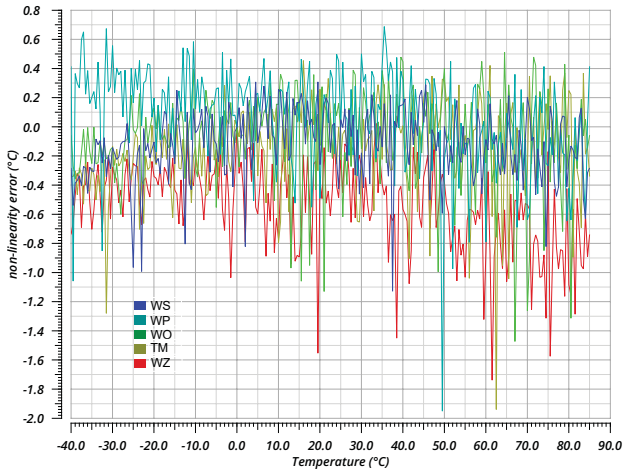

Figure 4 Temperature sensor nonlinearity error at VDD= 3.3 V and all possible process corners.

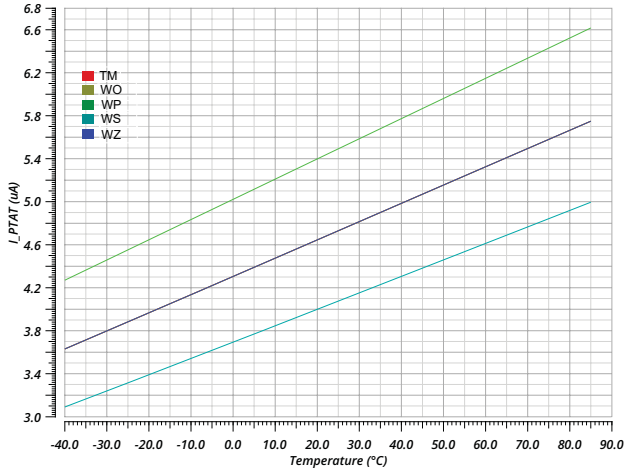

Figure 5 I_{PTAT} characteristics at VDD= 3.3 V and all possible process corners..

nominal conditions, while the sensor consumes 318 μW at the same condition. It is possible to reduce the power consumption by reducing the sensor frequency using larger capacitors/resistors. However, this will trade the design area, making this choice unsuitable for integrating more than one sensor on the same die. Another option is using a resistorless temperature-dependent nano-current source like the one proposed in [36]. However, the current-temperature linearity cannot be compared to the one based ΔV_{BE} solution presented in this design. Finally, the proposed sensor output signal frequency shows low sensitivity to the supply variation from 3 V to 3.6 V, where f_{OSC} changes only by 0.9 %.

4 Conclusion

In this paper, a 0.028 mm^2 quasi-digital temperature sensor based on ΔV_{BE} PTAT current source and simple current mode relaxation oscillator is designed using XFAB 0.35 μm. The achieved worst-case nonlinearity error of $-2.467\,^{\circ}$C for the temperature range from $-40\,^{\circ}$C to $85\,^{\circ}$C makes it a suitable candidate for an on-chip power monitoring systems with the possibility to integrate more than one due to its small size. Future work includes the insertion of the proposed sensor with other recently proposed non-intrusive sensors [37] to capture the dynamic variations of the system by using low-cost indirect measurement methods.

5 Literature

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