Integrated High Temperature Electronics for Sensors in Harsh Environments

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Abstract

As part of the Fraunhofer Lighthouse project "eHarsh" conducted by eight Fraunhofer institutes, a universal chipset was designed for the readout of sensors in harsh environments. The SOI-CMOS technology used was especially developed for high-temperature applications and allows operating temperatures of up to 300 °C. The chipset consists of an analogue sensor front-end IC for resistive sensors, a microcontroller and an interface IC. Measurements of the analog frontend IC show functional performance up to 300 °C and only aslight decrease of the measured SNR from 87 dB at 25 °C to 84 dB at high temperatures.

1 Introduction

1.1 Motivation

In the joint Fraunhofer Lighthouse project „eHarsh“ eight Fraunhofer institutes have focused on the development of sensor systems for ambient temperatures of up to 300 °C. Within the scope of the research are sensors [1], sensor electronics, packaging and accompanying material and device characterization as well as test and reliability simulations and analysis.

For signal conditioning, measurement control and interfacing integrated electronics were developed [2]. The overall goal was to design a modular high temperature capable chipset with a minimum set of necessary components to realize the full sensor electronics (Fig. 1).

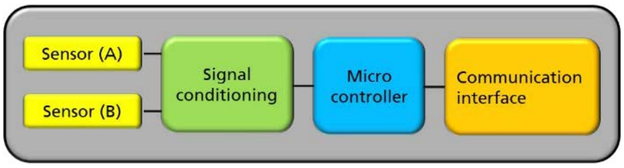

Fig. 1 Functional block diagram of the sensor system

Besides the integrated electronics only blocking capacitors are necessary as external components. Therefore, the typical elements of a sensor electronic are distributed over three chips, i.e. a sensor specific analog frontend, a Microcontroller and finally a sensor interface chip. All chips are designed in a high temperature 0.35-micron SOI-CMOS technology for a maximum target operating temperature of up to 300 °C.

1.2 High Temperature Technology

The technology used for the realized chipset is a 0.35 µm SOI-CMOS technology developed at Fraunhofer IMS, which is optimized for high temperature applications up to 300 °C [3]. Two gate oxides of different thicknesses are available for digital and analog transistors; wiring is supported by four layers of tungsten metallization. The technology has a wide range of standard analog elements like transistors, diodes, various resistors and capacitors. For digital designs, a standard cell library is available allowing netlist synthesis from a hardware description level as well as place and route of the digital system. Thus, automatic design is supported and principally every electronic function which is known from standard temperature range can be realized for high temperature environments.

With increasing complexity of integrated systems, there is an increasing demand for permanent storage of data. However, physically unavoidable charge loss is a severe limit for the data retention at high temperature. Because of this, commercial high temperature products only guarantee a data retention time of e. g. 1000 hrs. In this technology, a high temperature EEPROM is available showing a data retention of more than 10,000 hrs (measured at 250 °C). A special differential cell design has been implemented. The memory is typically used for permanent storage of calibration data, however, for applications with larger memory requirements, e.g. to store program code, also a variant with higher memory density has been developed.

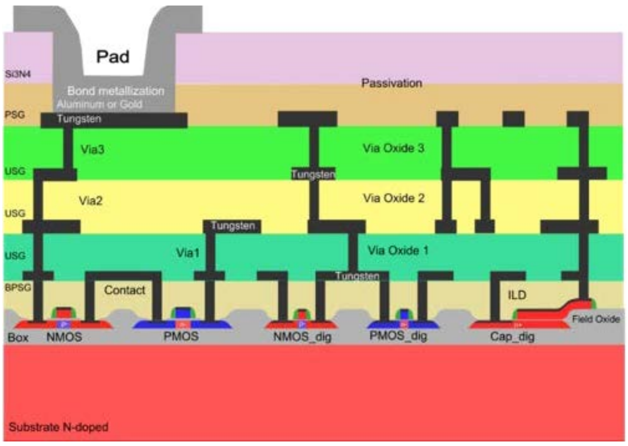

Fig. 2 Technology cross section of the Fraunhofer IMS High Temperature SOI-CMOS-technology H035

2 Integrated Chipset

The chipset described here contains three building blocks for typical sensor electronics. The analog frontend ASIC can be placed in close vicinity to sensor elements at high temperatures, thus allowing amplification, offset correction and analog to digital conversion with a high signal quality. Additionally, the supply and interface ASIC can be added which can locally generate internal supply voltages with a low distortion level. This chip also allows robust communication over an RS485 interface. Finally, for more complex tasks of control and signal conditioning in the digital domain, a microcontroller ASIC based on the RISC-V instruction set with various peripherals can be used. The three ASICs are described in the following chapters.

2.1 Analog Frontend ASIC (AFE)

For analog readout of sensors, a frontend chip was developed. This ASIC includes all functions to excite and readout resistive sensors, which have also been developed in the „eHarsh“ project [1]. It comprises three separate signal paths supporting simple resistive sensors as well as sensors in Wheatstone configuration. Each signal path is equipped with a programmable gain amplifier (PGA) with programmable integrated input offset and sensor bridge offset correction and a sigma delta converter (SDC) as depicted in Figure 3.

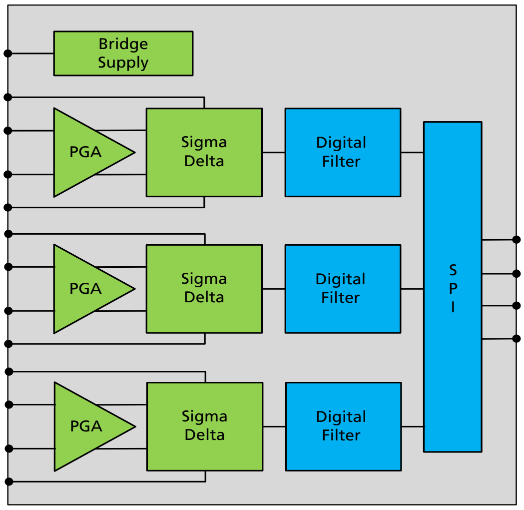

Fig. 3 Block diagram of the analog frontend ASIC

The input stages are built of a differential structure as common for an instrumentational amplifier. For cancelling of amplifier input offset and suppression of flicker noise the amplifiers are realized as auto-zero amplifiers. Additionally, the offset of a connected sensor bridge can be corrected internally. The gain of the amplifier is programmable to adapt the sensor bridge full scale swing to the sigma delta converter input range. After amplification and offset correction, the signal is fed differentially into the subsequent sigma delta converter.

Measurements of the signal to noise ratio (SNR) of the AFE ASIC have been made up to temperatures of 250 °C. Fig 4 shows the SNR over an input range of +/ - 1V with a nominal range of +/- 0.6 V. It can be observed that the SNR only slightly decreases with temperature.

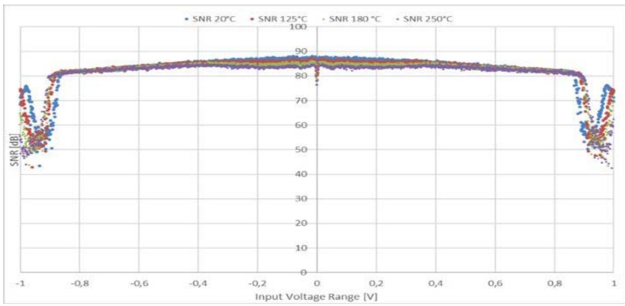

Fig. 4 Signal to noise ratio from 20 °C to 250 °C

Fig. 5 shows a chip photo of the AFE ASIC, realized in the Fraunhofer IMS high temperature SOI-CMOS technology H035. The chip size of the ASIC is 4.5 x 5.5 mm².

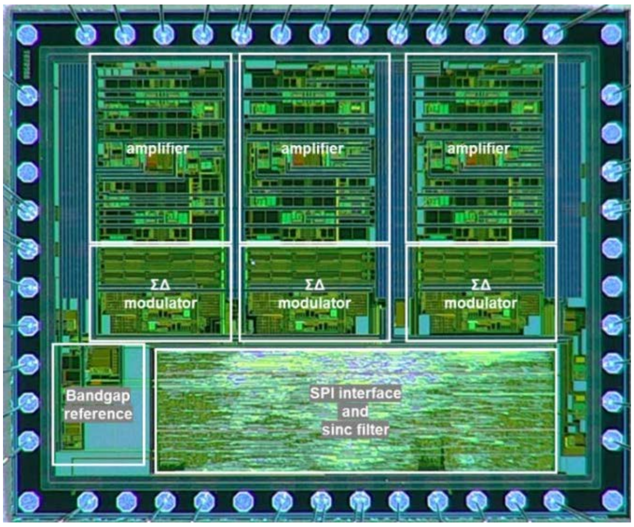

Fig. 5 Chip photo of the analog frontend ASIC

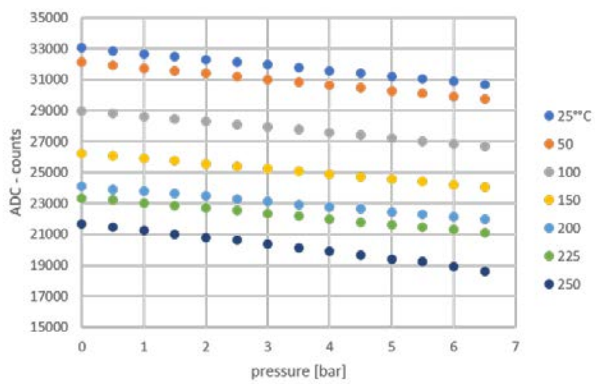

Fig. 6 Measurement of analog frontend ASIC with sensor bridge

In Fig. 6, measurements of the AFE -ASIC with the pressure sensor developed in „eHarsh“ up to 250 °C are shown.

ISBN 978-3-8007-5835-7

2.2 Supply ASIC

The supply and interface chip includes voltage regulators to supply the microcontroller and the analog signal path, respectively. The chip supports input voltages from 4.5 to 6.5 V. As reference an internal bandgap is used. In addition, the chip is equipped with an RS485 interface intended as a robust sensor bus interface.

Fig. 7 shows a chip phot of the supply ASIC, also realized in the H035 technology of Fraunhofer IMS. The chip size of the ASIC is 3.5 x 3.5 mm^2.

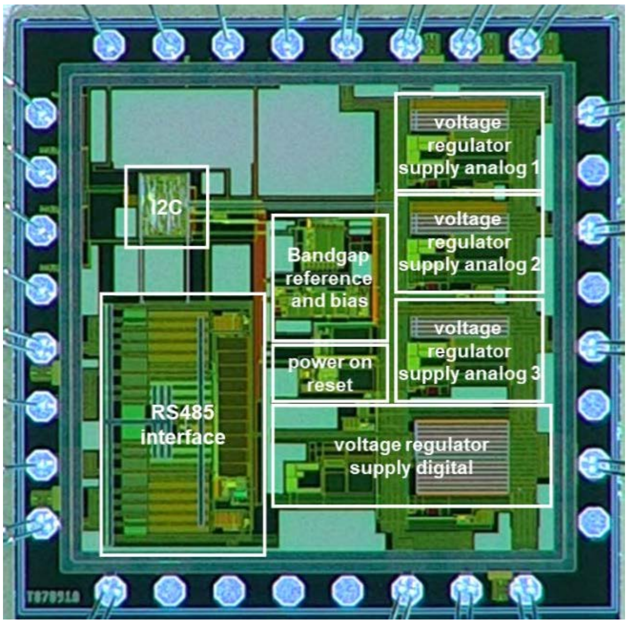

Fig. 7 Chip photo of the supply and interface ASIC

2.3 Microcontroller ASIC

For more complex tasks of signal conditioning and control, a 32-bit micro-controller has been developed. It is realized based on the RISC V instruction set (RV32IMC) supporting integer multiplication and division as well as compressed 16-bit instructions.

The microcontroller is equipped with standard peripherals like UART, SPI, I2C and timers. In addition, it includes a 12-bit SAR ADC. For code storage 16-Kbyte of High-Density-EEPROM have been developed. Further 4-Kbyte of RAM and a 512-byte EEPROM e.g. to store calibration data are included. Debugging of the processor is supported via a JTAG interface.

The system is implemented in such a way that it can later be expanded with little effort in terms of the number of processor cores (multi-core operation), memory blocks and peripherals. Figure 8 shows the block diagram of the controller which is currently in fabrication.

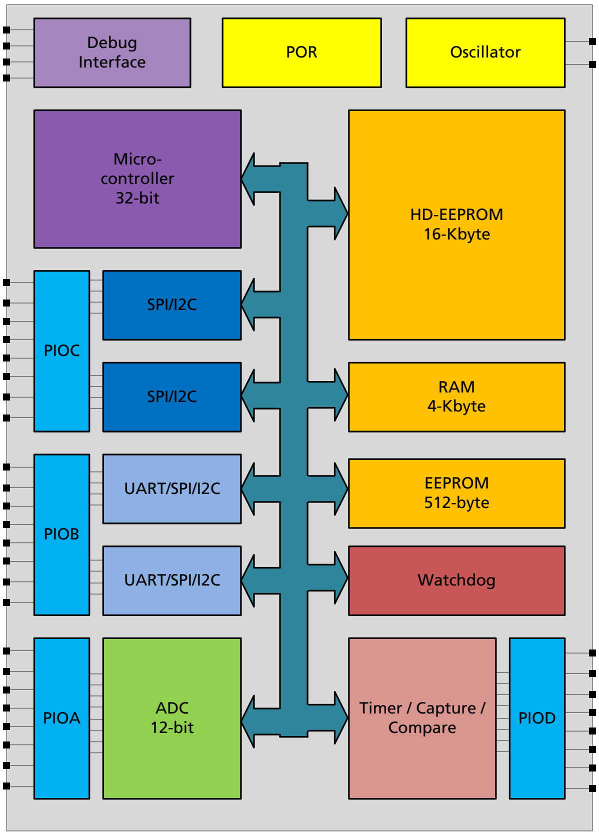

Fig. 8 Block diagram of the HT microcontroller

3 Conclusion

In this work, high temperature electronics for signal conditioning tasks in harsh environments has been pre sented. It has been demonstrated, that high precision analog signal conditioning as well as computing power in form of a microcontroller can be realized for temperatures up to 300 °C.

4 References

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ISBN 978-3-8007-5835-7