Low-Cost Efficient Indirect Power Monitoring Method for Optimization of Reconfigurable Analog Readout Circuits with Self-X Capabilities

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Abstract

In this work, an efficient indirect measurement method is presented to optimize the performance of sensory readout electronics with self-X (self-calibration, self-healing self-adaptation, etc.) properties. The low-cost test signals are applied to the device under test (DUT), and the output transient response is observed using total harmonic distortion (THD) to correlate the device's characteristics. Due to the search space complexity of the DUT, a population-based evolutionary algorithm is being used as an optimizer. Furthermore, a cost-effective indirect power monitoring scheme is being proposed to involve the power dissipation constraint during the optimization process. It helps to enhance system power efficiency, long-term reliability and insurance of accomplishing a safe reconfiguration pattern in the analog evolvable circuits. The feasibility of this approach is evaluated by a case study using an indirect current-feedback instrumentation amplifier on XFAB 0.35 µm CMOS technology. With the integration of the power monitoring module, the average power consumption of the DUT reduces roughly by 25% as compared to previously presented work in [1]. Results from the simulation test demonstrated the accurate estimation of the DUT characteristics from the low-cost test configuration with the average achieved THD value of -78.19 dB.

1 Introduction

Artificial intelligence (AI) and machine learning (ML) impact every aspect of life, such as computer vision, intelligent cars, robotics, understanding natural languages, industrial automation, and health diagnosis. Integrating AI and ML with evolving technologies, including edge computing, cyber-physical systems, big data analytics, and industrial internet of things, enables an immense transformation in the industrial field known as industry 4.0 [2, 3, 4]. The recent advancement in the computing power and digital revolution for a dramatic increase in data collection is initiating the revolution. This industrial revolution brings a massive era of information and understanding of the manufacturing space to increase productivity and reduce downtime. Smart sensors play a vital role in data generation in this new realm of industry 4.0 and IoT devices [5]. This data accuracy is essential for effective system performance estimation by ML or AI models. Instead, the decay of the performance of the measurement sensory electronics system is usually observed [6]. Analog integrated circuits are generally overdesigned to overcome this problem that consumes more power and occupy a larger area.

However, with the introduction of AI and ML, these smart sensory electronic systems (SSES) will have self-x (self-optimization, self-calibration, self-healing, etc.) properties [5, 7, 8]. It enables in suit calibration or online calibrations opportunities to calibrate SSES even after the device fabrication [9]. Generally, the calibration methods are realized by designing an integrated circuit with controllable calibration or tuning knobs and system performance measurements setup. Whereas implementing the recalibration of SSES comes with a bigger die area, larger parasites, and longer optimization time. To solve this issue, we recently proposed the reconfigurability limited to the sensitive elements [10], which significantly influence system performance. Likewise, the system performance measurement setup cost is also equally necessary for SSES, especially in terms of system complexity.

There are two primary classifications of the system performance measurement methods, depending on the evaluation principle of the desired characteristics. The first class uses on-chip direct measurement methods to evaluate the device performance characteristics [11]. This method is accurate and precise but increases the designing complexity and area [12]. In comparison, the second class utilizes indirect performance measurement methods based on the statistical, which simultaneously estimates several performance characteristics from simple test stimuli [12, 13, 14, 15].

For example, a multitone signal is applied to the operational amplifier in [15], and a time-domain transient response is being analyzed to predict the performance parameters such as input range, bandwidth, gain, phase margin and slew rate. To further improve the estimation accuracy, an alternative performance test flow based upon the two defect filters method is presented in [14]. A similar method is demonstrated in [13], in which the performance parameters of ICs is predicted by using a single test of envelope detecting. Another low-cost indirect measurement method based on non-intrusive sensors is presented in [12], where the sensor is electrically disconnected from the device under test (DUT). These low-cost sensors give an

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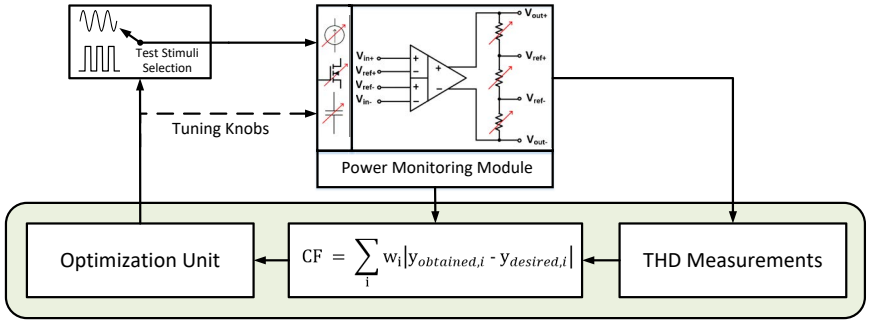

Figure 1 Block diagram of the proposed design methodology.

image of the operating conditions. As performance characteristics of ICs are strongly correlated with the operating conditions, the desired characteristics of the primary circuit can be easily predicted from cost-effective measurements of non-intrusive sensors.

Furthermore, power consumption is an elementary figure of merit in circuits design. One primary concern of the sensor nodes is the limited power resources, especially when deployed in not frequently accessible areas [16, 17]. However, with a proper power management scheme and configurable electronic hardware similar to the work presented in [18], these SSES can dynamically meet the desired performance with a minimum amount of power and increase the device's lifetime. Therefore, the primary objective of this work is to effectively optimize the performance of SSES using low-cost indirect measurement and power monitoring techniques.

2 Proposed Design Methodology

The block diagram of the proposed design is shown in the figure 1. Reconfigurable fully differential indirect feedback instrumentational amplifier (CFIA), which is an integral part of readout sensory electronics, is used as a test vehicle for the extrinsic evaluation of the proposed methodology. Tuning knobs are programmable arrays of capacitors, resistors, NMOS and PMOS transistors comprising binary-weighted scalable devices controlled by digital patterns generated by the optimization algorithm. For the selection of the optimization algorithm, the derivative-based optimizers cannot be used due to the discontinuous objective space [19]. On the other hand, meta-heuristic optimization algorithms perform considerably well even in the discontinuous objective space. Therefore, the recently proposed experience replay particle swarm optimizer (ERPSO) is utilized as an optimizer [1]. In ERPSO, the exploration capabilities of the traditional particle swarm optimization (PSO) have been expanded to satisfy the demands of the complex objective and search space of SSES. More details about ERPSO can be found in [1].

The test stimuli selection module includes the sinusoidal and step signals. The optimization algorithm firstly applied the sinusoidal signal to the CFIA. Then by performing the total harmonics distortion (THD) measurement at the sinusoidal response of the system, most of the performance characteristics can be easily predicted by using single execution. Since design imperfection such as input common-mode range (ICMR), slew rate (SR), gain-bandwidth, the effective number of bits (ENOB), full-power bandwidth, and SNR can be expressed as a nonlinear distortion at the output of the closed-loop amplifier. Though, the stability of the amplifier cannot be estimated by the spectrum analysis realized by the sinusoidal response. Hence, the stability of the CFIA is evaluated with the help of a step response.

The significant difference from our previous method [1] is the insertion of a power monitoring module (PPM). The PPM serves two essential purposes; firstly, it compares for the most power-efficient solution of the optimization algorithm. Hence, the power figure of merit will be optimized in the loop as well. Secondly, more importantly, check for the optimization pattern safety of the DUT. Unlike the optimization process of programmable digital devices like the field-programmable digital array (FPGA) or optimizing the feedback network of amplifiers and filters, optimizing the core amplifier may lead to a solution that fit the design performance at higher power. In some optimization solutions, the current flow may exceed the current density limit of the amplifier rails or the internal nodes. In a simple form, it causes a voltage drop on the supply lines or on the current-carrying connectors.

However, a severe degradation can occur due to the electromigration phenomenon in the connectors, leading to immediate chip failure or reducing the connection lifetime reliability, depending on the amount of current. Increasing the metal width to accompany the extreme current values is not a marvellous solution because it increases the layout area and introduces more parasitic coupling capacitors to sensitive nodes of the amplifier, eventually degrading the design performance after fabrication. In the conventional analog circuit design, the drawn current is well known and calculated according to the design requirements. Hence, the designer chooses the appropriate wire width during layout implementation by using the foundry process data books not to exceed the wire current density. Therefore, this work highlights the optimization of analog circuits by considering the chip reliability.

The proposed optimization flow diagram is presented in figure 2. It starts with the random initialization of the position and velocity of the particles. Firstly, the power consumption of the candidate solution from the optimization algorithm is evaluated. The optimization unit decides to

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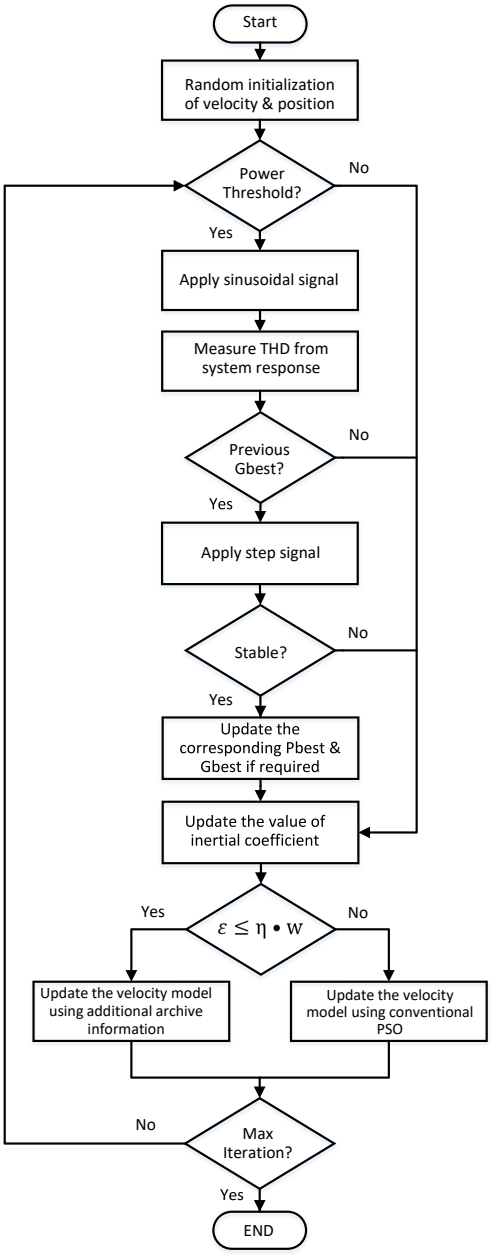

Figure 2 Flowchart of the proposed optimization algorithm along with power monitoring module. Where w is inertia weight, η denotes the intensity factor to control the exploration and exploitation, and ε is random variable for epsilon greedy algorithm.

pass or skip this solution based on the predefined threshold value. In the next step, the THD value is calculated from the reconfigurable amplifier output signal with the known sinusoidal fundamental frequency, and this THD and power consumption serve as a cost function or fitness value for the ERPSO algorithm. After that, the stability check of the CFIA is observed only in the case of a better fitness value obtained. In the next step, the velocity update equation of the traditional PSO is evaluated with the help of the previously visited global best minimum. The epsilon greedy algorithm is used to balance exploitation and exploration, and more details can be found in [1]. This process will continue until the maximum number of iterations.

3 Power Monitoring Module

A common approach for measuring the circuit current from the printed circuit board (PCB) community is by sensing the voltage drop on a tiny current-sense resistor (CSR) placed on the main path of the supply voltage using a differential amplifier and analog to digital converter [20]. Several factors have to be taken in this approach. Firstly, the voltage drop on the CSR should not effectively reduce the circuit headroom voltage when a high current is passing through it. Secondly, the resistor tolerances to the process variation and temperature drift should be ignorable for precision measurement, which is difficult to achieve using on-chip sheet resistors without trimming technologies. Thirdly, the CSR should be able to dissipate the developed power safely. In addition to the circuit complexity, the real issue of this approach is that it measures the power on the main supply rails that can be shared with different circuits having the same supply ring powered by the same power pads. Hence it is not possible by this approach to measure the power of the individual circuits unless individual power monitoring schemes are integrated and the supply rails and pads are separated, leading to more design constraints.

In some cases, detecting the threshold value of the power is only required, while measuring the absolute value is not of interest. For this purpose, authors in [21, 22] proposed a basic approach to detecting maximum power using a simple current sense sensor. Again, this approach shares the same problem of the former one by employing a current sensing resistor in the path of the supply rails. In this paper, we propose a simple alternative approach to indirectly estimate the current drawn of the configurable CFIA circuit by mirroring a scaled-down value of the circuit current into the current-starved ring oscillator [23] as shown in figure 3 (for simplicity, the biasing circuit, common mode feedback circuit and the current-starved oscillator circuits are not presented in the figure). Hence, modulating the drawn current and consequently the power dissipation in the form of clock frequency. The already available digital processing unit in smart sensory electronics can easily read the generated signal. Since the output frequency is proportional to the drawn current, this approach can detect the power threshold value and reasonably approximate the power estimation of different optimization solutions.

4 Results and Discussions

The performance of the proposed methodology is extrinsically assessed on the complex objective space of the CFIA circuit. For this work, a sinusoidal signal with a frequency of 100 kHz and amplitude of 2 V_{p-p} is used as a test stimulus for the desired THD of -70 dB. The sine wave signal is generated from the Cadence tools. Nevertheless, we have already started implementing a sine signal generation by utilizing the direct digital synthesizer circuit formed on the sine-DAC architecture [24]. For the step response test, we used a pulse signal with a period of 1 µs and an amplitude of 2 V_{p-p}. However, non-idealities of the assessment unit are not considered in this experiment for simplicity. The

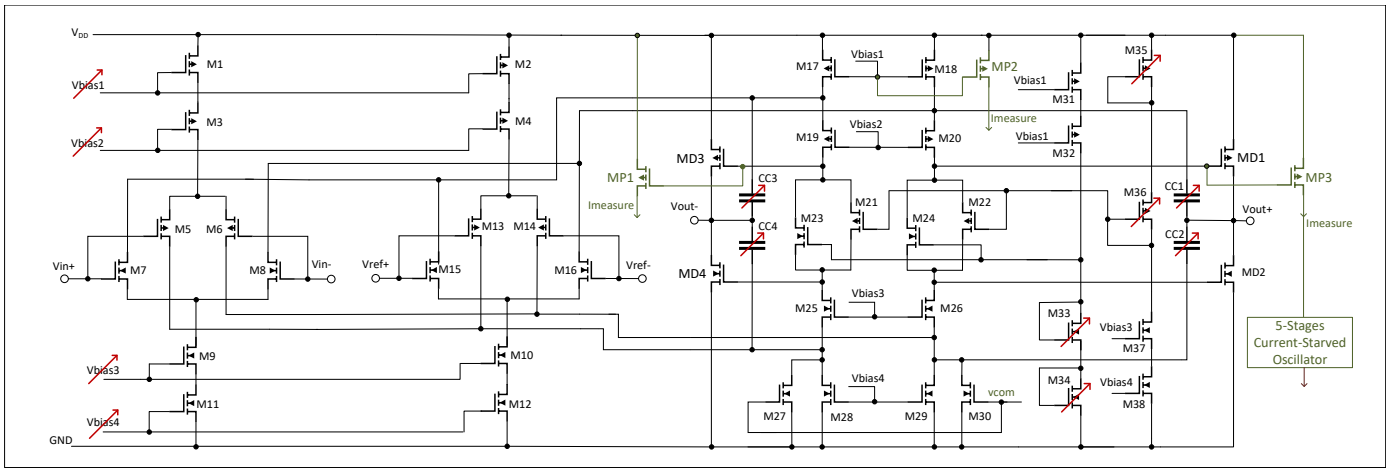

Figure 3 Transistor level schematic diagram of CFIA along with power monitoring sensor.

Table 1 Optimizied CFIA characteristics results.

CFIA design parameter	PVT Corners			Statistical Information		
	C_0	C_1	C_2	Mean	Min	Max
Differential DC gain (A_{VD})	96.18 dB	89.81 dB	93.92 dB	91.33 dB	88.13 dB	98.97 dB
Gain bandwidth product (GBW)	60.31 MHz	49.15 MHz	43.11 MHz	67.21 MHz	46.93 MHz	87.48 MHz
Phase margin (PM)	78.75°	67.17°	76.03°	72.13°	66.81°	80.34°
Slew rate (SR)	±69.16 V/µs	±61.29 V/µs	±45.12 V/µs	±73.81 V/µs	±59.17 V/µs	±85.28 V/µs
Total harmonic distortion (THD)	−80.16 dB	−77.13 dB	−76.46 dB	−78.19 dB	−81.37 dB	−76.11 dB
Static power dissipation (P_D)	5.85 mW	6.10 mW	8.13 mW	6.91 mW	5.12 mW	9.61 mW

ERPSO adjusts the width of sensitive elements as specified in [1], while lengths of transistors are kept constant to minimize channel length modulation effects. The transistors sizing information can be found in table 2.

The targeted power threshold is set according to the maximum safe current of 6 mA in the CFIA, which indirectly corresponds to the frequency of 1.3 MHz at the output of the PMM. In this work, we used Python language to implement the ERPSO and Cadence virtuoso OCeaN for the circuit simulation. The achieved performance characteristics after the optimization are summarized in table 1. The optimization is performed with C_L = 10 pF, R_L = 10 kΩ, and unity gain configuration. The proposed optimization methodology is tested under the nominal process, voltage, and temperature (PVT) conditions (C_0: Process = typical mean, V_{DD} = 3.3 V, T = 27 °C). Furthermore, it is examined under the worst-case PVT conditions (C_1: Process = slow corner, V_{DD} = 3 V, T = -40 °C, C_2: Process = fast corner, V_{DD} = 3.6 V, T = 85 °C).

As shown in table 1, the proposed design methodology effectively optimizes the DUT mainly for the THD and power and satisfies all its performance parameters. The optimization process runs the step response only if the swarm finds the global best particle to validate the solution stability. The optimization process usually only performs the sinusoidal response, resulting in a further decrease in design automation time. The optimization run is repeated over five times, and the statistical information of the optimization process for the typical mean condition is shown on the right side of table 1. For this test, the performance parameters of the CFIA are extracted from multiple optimization results based on the specified THD value. As it can be observed from this table, the power consumption of the CFIA is far below the threshold value, and with the help of target THD value, it satisfies the characteristics of CFIA.

Table 2 MOSFET size ratios of the CFIA circuit.

Tr. Nr.	(W/L) [µm/µm]	Tr. Nr.	(W/L) [µm/µm]
M1, M2	256/1	M21, M22	52/0.55
M3, M4	128/0.5	M23, M24	18/0.55
M5, M6, M13, M14	120/0.7	M25, M26	42/0.7
M7, M8, M15, M16	40/0.7	M25, M27-M30	50/1
M9, M10	40/0.5	M31	64/1
M11, M12	80/1	M32	32/0.35
M17, M18	300/1	M37	10/0.5
M19, M20	132/0.7	M38	20/1
MD1, MD3	240/0.35	M33*, M34*	64/0.5
MD2, MD4	80/0.35	M35*, M36*	128/0.5
MP1-MP3	1/0.35		

where * represents scalable devices.

5 Conclusions

The main contribution of this work is to present the low-cost indirect performance and power monitoring method for reconfigurable readout sensory electronics systems. The efficiency of the proposed methodology is illustrated extrinsically by attained performance parameters of the CFIA. The THD-based indirect performance evaluation methodology is being utilized to optimize all reconfigurable SSES at once. Furthermore, the proposed power monitoring module helps to optimize for the power-efficient solution and safe reconfiguration pattern for the

DUT. With the introduction of PMM, the average power consumption of the typical mean condition compared to previously presented work [1] reduces nearly by 25%. However, other characteristics, especially GBW and SR, were slightly decreased but still satisfying the targeted THD value. For future work, the algorithmic part of the proposed methodology will be implemented by using FPGA and the fabrication of reconfigurable CFIA research chip is targeted, as a baseline step towards advanced USIX (universal and Self-x integrated sensor interface) chip [25] to provide a hardware platform for SSES with self-x properties for industry 4.0.

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